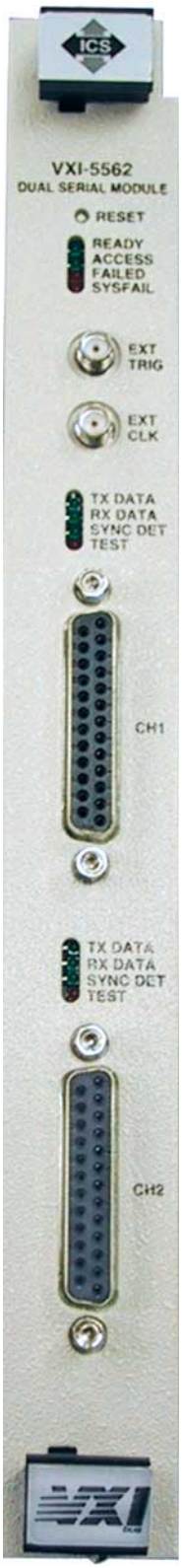
VXI-5562

DUAL BINARY SERIAL MODULE



DESCRIPTION

The Model VXI-5562 Dual Channel Serial Module is a single slot, C-size VXI module with two channels for sending and receiving serial binary messages at rates up to 9 Mbs. Each serial channel has large FIFOs for buffering transmit and receive data. The channel's transmit and receive logic has multiple operating modes that let it create many serial protocols and duplicate other serial devices. Each channel can transmit and receive data with various combinations of clock and data-gate signals through RS-422 or LVDS interfaces. The serial clock for both channels can be supplied by an internal frequency generator or by an external clock from an SMA connector on the module's front panel. The VXI-5562 is a register based VXI module and can transfer data at rates up to 16 Mbs over the VXIbus. Applications include test systems or command and telemetry applications.

Serial Interface Organization

Each serial channel provides transmit data, transmit clock, and transmit enable signals as its outputs. Channel inputs are receive data, receive data clock and receive enable signals. User selects the RS-422 or LVDS transceivers for each channel. The standard module has 100 ohm load resistors on all receiver and zero ohm series resistors for the RS-422 transmit signals.

Transmit Data Modes

The VXI-5562 has multiple modes for transmitting binary data. Data transmission can be continuous as long as there is data in the Tx FIFO or it can be a series of single message packets. Continuous data transmission can start when data is placed in the transmit buffer and when the continuous transmit line is asserted. Single messages can be individually sent by momentarily asserting the single transmit line or by triggering the channel. The channel can be triggered by a selected VXI TTL Trigger or by an external trigger from the module's front panel. The module can automatically send a message after it has received a message when the Tx-on-Rx line is asserted.

Data messages can be transmitted with a continuous clock output or with a gated clock output with one clock for each data bit. Data transition occurs on the positive going clock edge. The enable line output can be continuous high or gated so that it is high when data is being transmitted. The transmit data line can be quiet between messages or fill data messages can be automatically inserted when the Tx FIFO becomes empty. When fill data is being sent, data transmission restarts at the end of a fill message when new data is available.

Transmit FIFO

Data is loaded into the channel's transmit FIFO as a series of 16-bit words. The last word of a message is marked by a separate end bit in the Tx FIFO. If the messages are multiples of 16-bit words, the next message starts with

- Sends and receives 16-bit word and arbitrary bit length messages with baud rates up to 9 Mbs.
  Handles most binary formats at high transfer rates.
- Multiple transmission modes and programmable gate and clock outputs.
  Duplicates most serial protocols.
- Receiver inputs data upon command or when a sync pattern is detected.
  Captures both types of messages.
- Register based interface has fast VXIbus data transfer rate
  Reduces VXIbus transfer time.
- Large Tx and Rx FIFOs hold 2 Mbytes.
  Enough data for a complete test sequence.
- Internal Baud Rate Generator covers a 1 to 10 MHz range
  Provides all clock rates.
- Transmission can be triggered with external or VXIbus triggers.
  Easily controllable in a test system.
- Custom protocols with special firmware.
  Adapts module to your special test needs.

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the next word. If the messages are not multiples of 16-bit words, the user supplies a count word to tell the module how many bits of the last word are to be transmitted. The next message starts after the count word. If the message is a multiple of the 16-bit data words, then the VXI-5562 can add a 17th odd or even parity bit to each 16-bit word. The Fill FIFO has the same format as the Transmit FIFO

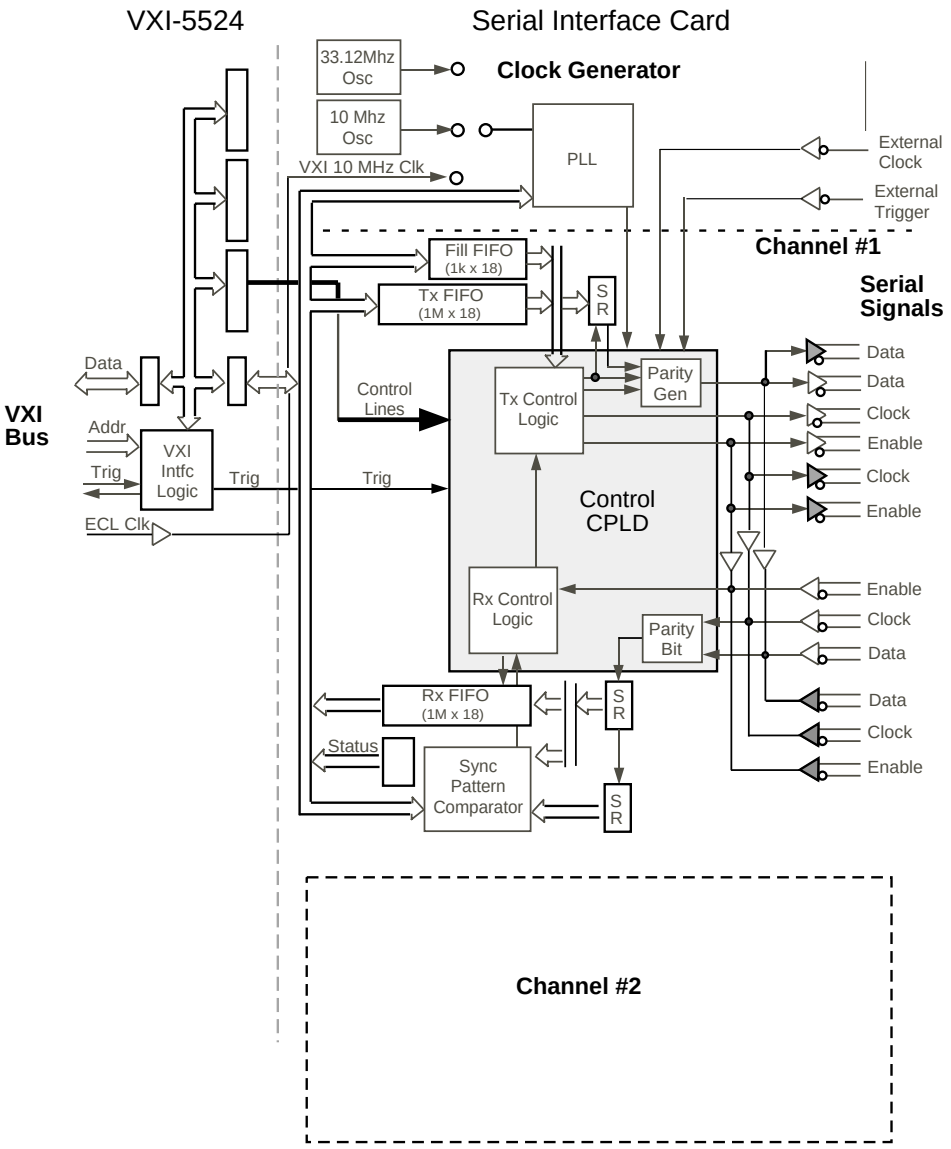
Receiver Operation

Received data can be captured upon command or when a 8, 16, 24 or 32-bit sync pattern is detected. If sync is enabled, the user stores the sync pattern in the receive channel before enabling the receiver. Data capture will start with the bit immediately following the sync pattern. If Gated Enable is selected, data capture starts when the leading edge of the data gate is received. If Gated Clocks are selected, data capture starts when the first clock pulse is received. While data is normally sampled on the falling edge of the clock signal, it can be sampled on the positive going clock edge.

Received data is stored in the VXI-5562's Rx FIFO as a series of 16-bit words. When parity is enabled, the received parity bit is saved as bit 17 in the Rx FIFO. The first word of each message is marked by writing a 1 to bit 18 in the Rx FIFO. Residual data that is left in the receiver when the receive clock stops is lost. The received data is held in the Rx FIFO until it is read by the VXI Controller.

VXI Bus Interface

The VXI-5562 Dual Channel Serial Module is a register based module with D16 data capability. Transmit and receive data is transferred over the VXI bus is as 16-bit wide words at a 16 Mbits per second rate. Transmit date is written directly to the Tx FIFO and is read from the Rx FIFO. Both the Tx and Rx FIFOs each hold 2 Mbytes of data. The Fill FIFO holds 1024 bytes. A status byte word lets the user read the status of the FIFOs in each channel and the parity and new message bits from the Rx FIFO.



Program Capability

The VXI-5562 uses 16-bit binary words written to command registers to set each channels' operating modes, to set the internal transmit clock rate, to select the clock and trigger sources and to select the RS-422 or LVDS differential transceivers.

Data is typically loaded into the Tx FIFO before starting data transmission. For continuous operation, data can be loaded into the Tx FIFO while the unit is transmitting as long as the VXI Controller can keep up with the VXI-5562's data transmission rate. When Fill is enabled, the user can turn off the Continuous Tx enable while loading data without interrupting the fill data. Data transmission will start at the end of the next fill message when the Continuous enable line is reasserted.

Each channel can be set to interrupt the controller when data is first received or when the Rx FIFO overflows.

Custom Protocols

The VXI-5562 can be modified for custom protocols by changing the code in the CPLDs. Contact ICS for information about implementing your protocol in the VXI-5562.

VXI Capabilities

Static address capability.
Register based instrument.
A16 address space.
D16 bit data.
Normal handshake data transfer.

Diagnostic Capability

Includes internal and external data loopback and front panel LEDs for VXI status and troubleshooting.

Transmission Modes

Each channel has the following transmit modes:

- 16-bit word messages
- Arbitrary length messages
- Continuous transmission
- Single message transmission
- Trigger Enabled transmission
- Transmit on received message
- External trigger/VXI trigger select
- Gated Enable signal
- Gated Tx clocks
- Fill enable
- Parity bit enable
- Odd/Even Parity Select
- RS-422/LVDS drivers select

Receive Modes

Each channel has the following receiver modes:

- Receive enable
- Sync detect enable
- 8/16/24/32 bit compare select
- Positive Rx clock

Test Modes

Each channel has the following test modes:

- Clock and Enable loop back
- Data loopback
- External loopback

Serial Interface

Transmits and receives serial bit streams. Transmit/receive logic supports RS-422 and LVDS interface drivers and receivers. Receiver inputs data upon command, when gate or clock received or when sync pattern detected.

Serial Signals:

Transmit	Data, clock, and enable
Receive	Data, clock and enable.
Signal type	Differential RS-422 or LVDS signals.

TX Rate
Maximum rate depends upon selected transmission options.

- 16-bit word messages > 9 MHz
- Arbitrary length messages > 5 MHz
- Fill Enabled >5.9 MHz

Message lengths :

- Data 2 to 2 Mbytes

Data Timing

- Tx Data bit change on positive clock edge
- Rx Data read on negative or positive clock edge

Trigger Sources

- VXIbus TTL Trigger line 0, 2, 4, or 6.
- Front Panel triger pulse into a 50 ohm load

Clock Sources

- Internal clock derived from internal oscillator or VXI 10 MHz clock.
- Front Panel clock input into a 50 ohm load

Sync Detector 8, 16, 24 or 32 bits

FIFO Data Storage

Each serial channel has separate transmit, receive and fill FIFOs

Data FIFOs	2 Mbytes
Fill FIFO	1,024 bytes

Internal Clock Generator

Frequency synthesizer type generator based on internal 33.12 MHz oscillator or VXIbus 10 MHz reference. The Internal Clock Generator is programmable from 1 to 10 MHz.

Physical

Size, W x H x D
C-sized module
(30.5 x 233.5 x 353.0 mm)

Weight
2 kg. (.4.5 lbs.)

Power Consumption
+5 Vdc at 2 Amperes

Connectors

Serial:	DB-25S connectors with lock studs/Ch
Ext Trigger:	SMA connector/Ch
Ext Clock:	SMA connector

Indicators

Common LEDs:
PWR, ACCES, FAILED and SYSFAIL

Channel LEDs
TX DATA, RX DATA, SYNC DET and TEST MODE

Included Accessories

Instruction manual

ORDERING INFORMATION

	Part Number
VXI-5562 Dual Channel Serial Interface	VXI-5562